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A Si nano–micro-wire array on a Si(111) substrate and field emission device applications

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Abstract

A large number of Si wires on Si(111) can be fabricated selectively by the vapor–liquid–solid growth method with a high aspect ratio greater than 100. The diameter of the wire can be controlled from less than a micron to a few hundred microns. We propose a novel smart field electron emission device using silicon nano-wires fabricated by this vapor–liquid–solid growth method, and demonstrate field electron emission with a quite low operation voltage from a gated silicon nano-wire. The threshold voltage is about 13 V, and the value is similar to those for gated carbon-nanotube field emitters. The emission current reaches 10 nA at 15 V gate voltage.

Keywords: VLS growth; Nano-wire; Field emission; Si integrated circuits

1. Introduction

Recently, electron field emission from a variety of nanostructures such as carbon nanotubes [1], porous Si [2], roughened Mo [3], nano-protrusions on iridium [4] and silicon nano-protrusions [5, 6], has attracted much attention as regards application in displays and other vacuum electronic devices working under low applied voltages. Several literature reports concerned gated carbon-nanotube field emitters, and their threshold voltage is around 10 V [7, 8].

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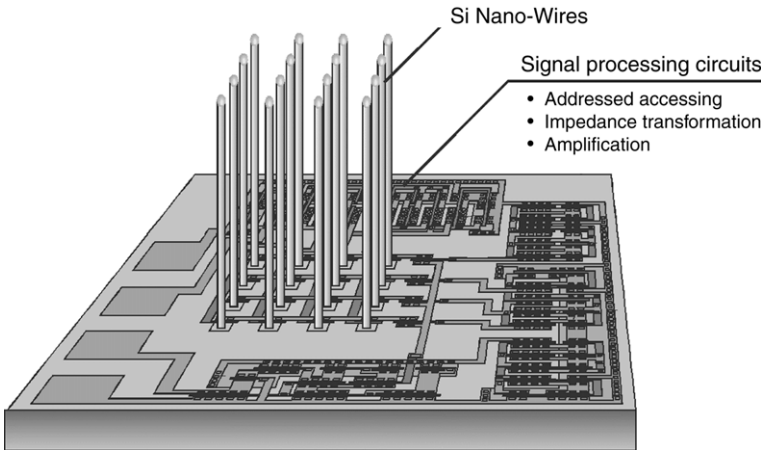

Fig. 1. The schematic structure of a pixel of the proposed smart field electron emission device using silicon nano-wires.

Silicon field emitter arrays (FEAs) are attractive candidates for vacuum microelectronics applications because of the possibility of monolithic integration with various circuits [9]. When we fabricate a smart electron emission device which is constructed with a Si solid-state LSI (large-scale integrated circuit) part and an electron emission device part, non-Si electron emission materials are difficult to combine with Si integrated circuits.

If the silicon field emitters operate at less than 10 V, a fused electron device, combined with a vacuum device with a Si LSI, can be realized. In this paper, we present field emission properties of a Si nano-wire with a very low threshold voltage ($V_{th} = 13$ V). The nano-scaled single-crystal Si wires, which can be controlled as regards position, density and size, were grown by the selective VLS (vapor–liquid–solid) growth method on a Si substrate. We have already demonstrated growth of Si wires on Si circuits.

2. Selective VLS growth

The schematic structure of a pixel of the proposed smart field electron emission device using silicon nano-wires is illustrated in Fig. 1. For the smart field electron emission devices, we propose a field emitter array with on-chip MOSFET circuits for signal processing, using selective VLS growth of the Si probes after the MOSFET IC process [10].

Previously, we demonstrated growth of a variety of single-crystal Si wires on Si substrates by using the VLS growth method, and they are applicable in neural activity recording systems [10]. For fabricating a Si probe array on the Si wafer, the VLS process was a key technology. The position, density and size were well controlled for changing growth conditions [11]. It is well known that the growth direction of the Si wire is ⟨111⟩ in VLS growth, and Au dots on the Si wafer become Au–Si alloy droplets and remain at the tip of the Si wire during the VLS growth, which results in a high aspect ratio of the Si probes; so the on-chip MOSFET circuits must be fabricated on Si(111) surfaces. From

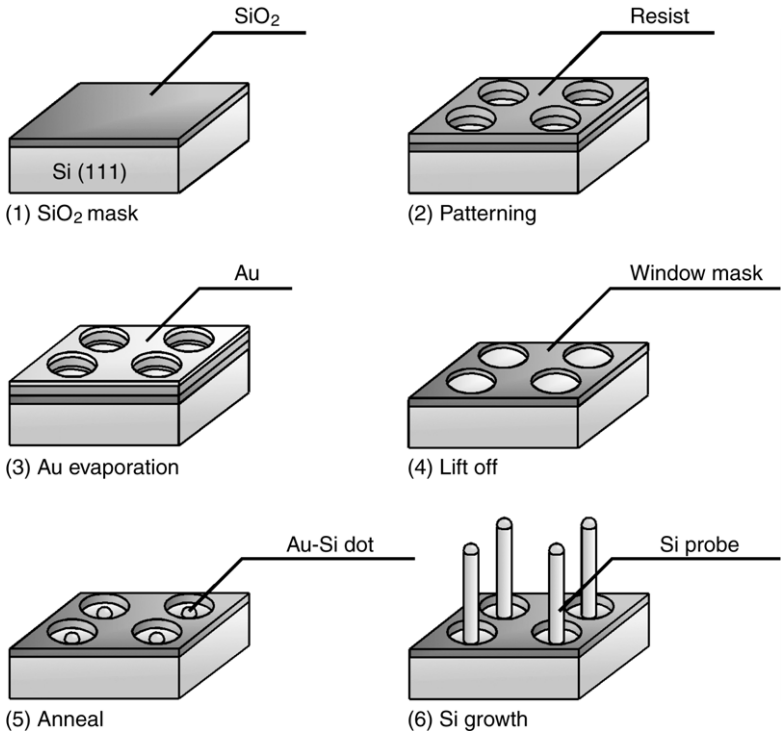

Fig. 2. The Si nano-wire fabrication process. The Si nano-wire is grown by a selective VLS growth method.

previous results of our studies, MOSFET fabrication after the VLS Si wire fabrication process was carried out successfully.

3. Experiment and result

3.1. Field electron emission from Si nano-wires

For field electron emission devices, the desired tip diameter of the Si nano-wires must be less than 100 nm, and the aspect ratio will be higher than 10. The diameter of a typical multiwall carbon nanotube is about 60 nm. The VLS method enables one to control the size and the position of Si probes using a SiO_2 window mask and a lift-off process, by photolithographic techniques.

VLS growth of the Si wire probe was carried out on a Si(111) substrate using Au dots formed by a lift-off process followed by Si_2H_6 gas source MBE (molecular beam epitaxy). Fig. 2 illustrates the Si nano-wire fabrication process. First, a SiO_2 mask was formed and patterned on the Si(111) wafer. The SiO_2 windows were opened by HF solutions, and the diameter was 200 nm. The resists were patterned using an electron beam lithography system. Then an Au film with 160 nm in thickness was evaporated over the photoresist on the patterned SiO_2 window mask. After removing the Au on the photoresist

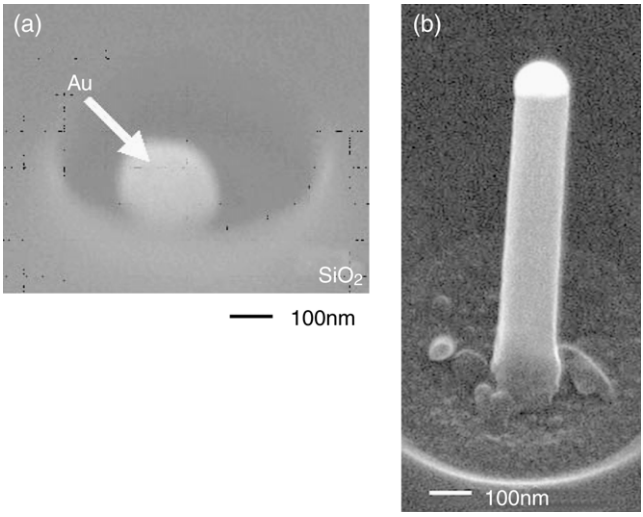

Fig. 3. An SEM photograph of an Au–Si alloy droplet; the diameter of the droplet is about 100 nm (a), and an SEM photograph of the Si nano-wire (b). Single-crystalline Si probes grow perpendicularly to the Si(111) wafer. The diameter of the Si nano-wire was 120 nm, and its length was 1.4 μm.

by a lift-off process, Au dots remained at pre-determined Si nano-wire sites, where the Si surface was revealed by the patterned SiO_2. The wafer was introduced into the GS MBE chamber and annealed to form Au–Si alloy droplets. The annealing temperature was 600 °C, and the time was 5 min. An SEM photograph of a Au–Si alloy droplet is shown in Fig. 3(a). It is found that the diameter of the droplet is about 100 nm. Si_2H_6 gas was introduced into the chamber at the growth temperature of 650 °C. The Si_2H_6 gas causes the Au–Si droplets to be supersaturated with Si, which results in precipitation of Si atoms at the interface between the alloy droplet and the Si wafer. As shown in Fig. 3(b), single-crystalline Si nano-wire grows perpendicularly to the Si(111) wafer surface, with a Au–Si alloy dot at the tip. This shows that the Si nano-wire was formed by selective epitaxial Si growth, and the nano-scaled Si wire was successfully grown. The diameter of the Si nano-wire was 120 nm, and its length was 1.4 μm. The diameter and spacing of the Si probes can be controlled by changing the patterned Au dot diameter and spacing, respectively.

First, emission characteristics from the Si nano-wires were measured in a diode structure without gate electrodes for simplicity. The base pressure of the chamber during measurement was 3×10^{-6} Pa. The distance between the anode and the chip of the n-type field emitter array was kept at 10 μm. The Si wafers were grounded and the anode was biased from 0 to 1200 V. Typical field emission characteristics for 100 Si wires are shown in Fig. 4. The emission current was observed from the anode voltage of 580 V, and the emission current reached 1 μA at the anode voltage of 1150 V. The Fowler–Nordheim (FN) plot shows the typical characteristics of field emission, and it is likely that the Si nano-wires acted effectively as field emitters.

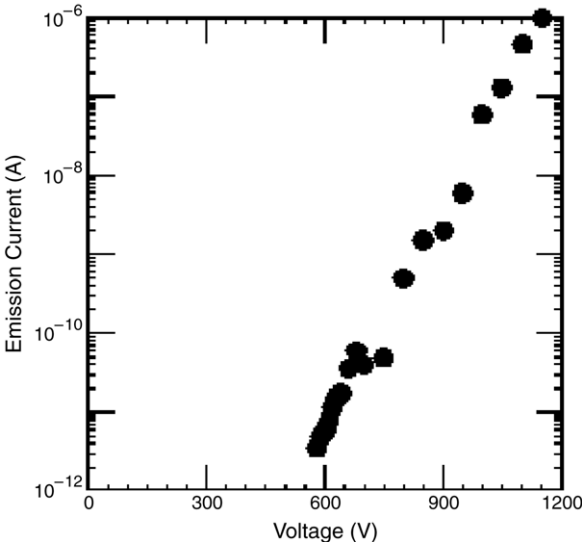

Fig. 4. Field emission characteristics for Si nano-wire.

During the Si nano-wire fabrication process, many kinds of Si nano-wires were observed. To change the growth conditions or annealing conditions, some kinds of crowded nano-wires were grown. Fig. 5(a) and (b) shows typical crowded nano-wires. The smallest radius of the apex of the nano-wire in (a) was about 22 nm, and that of the nano-wire in (b) was 31 nm. These nano-wires are not uniform and the numbers of nano-wires are also different. The number of wires in Fig. 5(a) is 144, while in Fig. 5(b) it is 37 500.

Field emission characteristics of these crowded nano-wires were measured. Fig. 6(a) and (b) show emission current characteristics of two types of nano-wire (Fig. 5(a), (b)). The threshold field of the field emission from Si crowded wires (Fig. 5(a)) is about 0.5 V/μm. The threshold voltage is lower than that of field emission from typical carbon nanotubes. (The conventional threshold voltage of a carbon nanotube is about 1.5 V/μm.) The apex curvatures of the Si nano-wire tips and the carbon nanotubes are almost the same. The threshold of the nano-wire in Fig. 5(b) is higher than that of Fig. 5(a). We suppose that the threshold voltage is strongly dependent on the apex curvature. The FN plots of these field emission currents show typical characteristics of field emission.

3.2. Nano-silicon field emitter with gate electrode

To operate the Si field emitters under low operating voltage (lower than 10 V), triode-type field emitters are indispensable. Recently several literature reports concerned gated carbon-nanotube field emitters, and their threshold voltage is around 10 V [7, 8]. However, integration of a carbon nanotube and a Si LSI is very hard. Triode-type field emitters using Si nano-wires were fabricated by the VLS method. VLS growth was carried out on a patterned poly-Si/SiO_2/Si substrate as shown in Fig. 7. Electron beam resist was coated on the substrate, and was patterned using an electron beam lithography system.

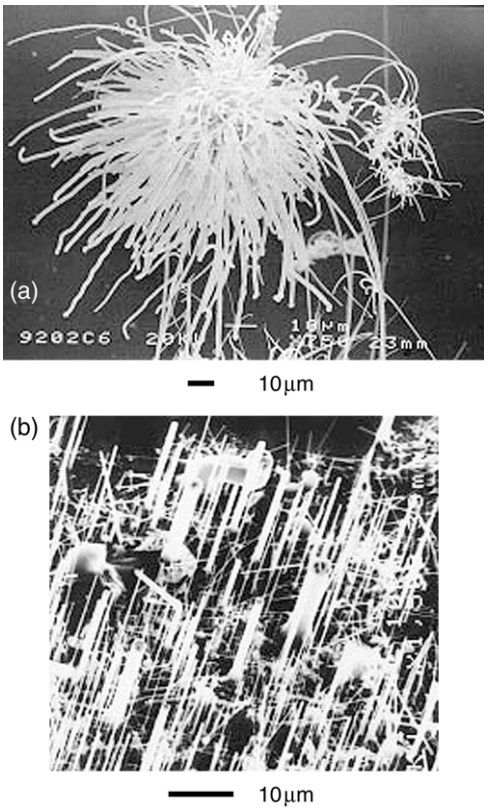

Fig. 5. Typical crowded nano-wires. They were grown to change the annealing temperatures or growth temperatures.

The thicknesses of the SiO_2 and phosphor doped poly-Si films are 1 μm and 300 nm, respectively. The poly-Si and SiO_2 film were patterned circularly on a Si(111) wafer, and their diameter was 200 nm. The poly-Si film was etched by RIE (reactive ion etching), and the SiO_2 windows were opened by HF solutions.

Gated single-crystal Si nano-emitters were successively grown on Si substrates as shown in Fig. 7. In the Si nano-wire growth process, the substrate temperature was kept at 600 °C, and the growth time was 3 min. From the fabricated triode-type field emitter of Si nano-wire, field electron emissions were successively observed at low gate voltages, and the electrical characteristics ($I_{emission}$–V_G) are shown in Fig. 8. The diameter of the Si nano-wire was 90 nm and length was 900 nm. The threshold voltage was about 13 V, and this value is similar to that for a gated carbon-nanotube field emitter (the reported lowest threshold carbon-nanotube emitter) [8]. The emission current reached 10 nA at 15 V gate voltage. Gated CNT emitters, reported previously, were constructed from several thousand CNTs, but our Si emitter contains only one.

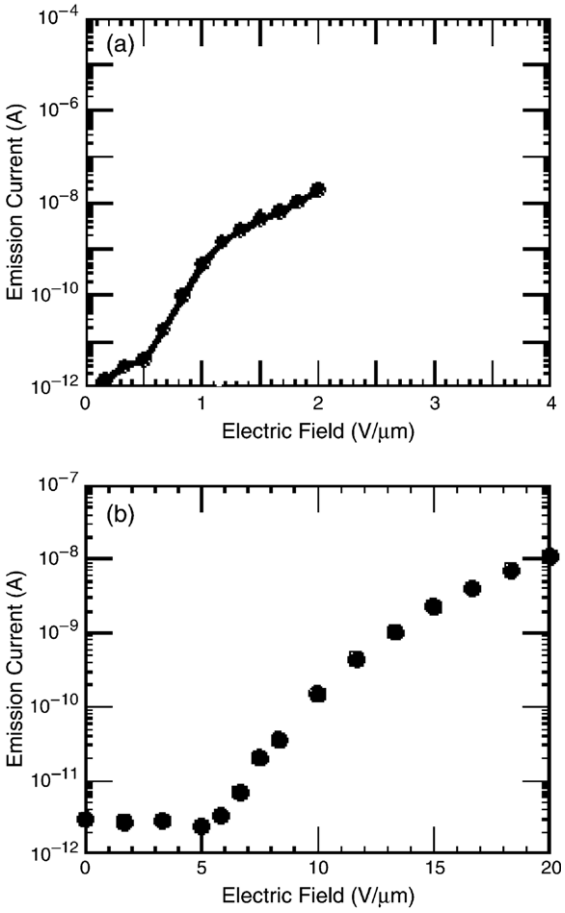

Fig. 6. Field emission characteristics of crowded Si nano-wires.

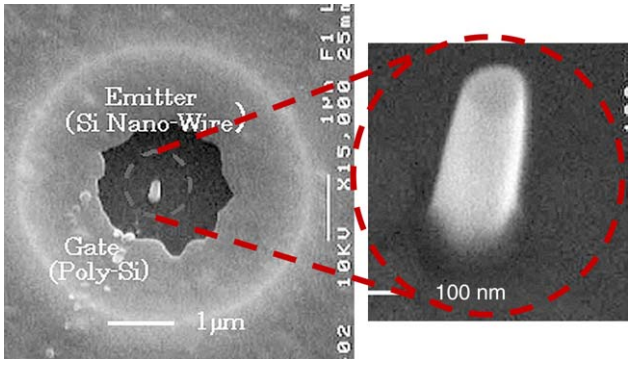

Fig. 7. Gated single-crystal Si nano-emitters were successively grown on Si substrate. The diameter of the Si nano-wire is 90 nm and the length is 900 nm.

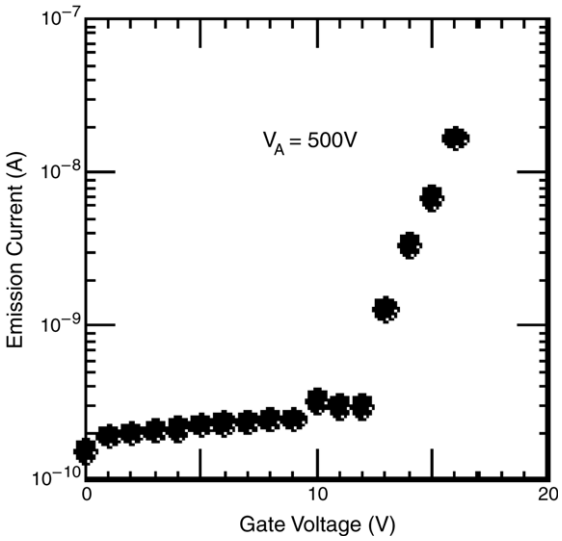

Fig. 8. The threshold voltage of the Si emitter is about 13 V. The emission current reaches 10 nA at 15 V gate voltage.

4. Conclusion

A large number of Si wires with a high aspect ratio greater than 100 can be fabricated selectively by the vapor–liquid–solid growth method. The diameter of the wire can be controlled from 90 nm to several hundred microns. We reported field electron emission from a gated Si nano-wire. The field emission characteristics were investigated and the threshold voltage is similar to that of a gated CNT emitter, which has the lowest threshold voltage for a CNT reported in the literature. We believe that a Si nano-wire with a Si LSI is an attractive candidate for use in smart field emitter devices.

Acknowledgements

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